41. The circuit of claim 40 further comprising a second control pin separate from the serial pin, information indicating when an end of frame has occurred being presented on the second control pin.

42. The circuit of claim 37, further comprising a control pin separate from the serial pin, information presented on the first control pin indicating a synchronous modem transmission protocol event.

43. The circuit of claim 42, the synchronous modem transmission protocol event indicating an end of frame.

44. (Amended) The circuit of claim 42, the synchronous modem transmission protocol event indicating when the modem is ready to accept additional data from the interface.

45 The circuit of claim 37, further comprising at least one control bit within words presented on the serial pin, the at least one control bit indicating a synchronous modem transmission protocol event.

46. The circuit of claim 45, the synchronous modem transmission protocol event indicating an end of frame.

## REMARKS

Status of Claims

Claims 1, 5-7, 9, 23, 26, 30, 37, 40, 44 have been amended to clarify the claimed invention. Claims 1-46 are now pending in the case.

Additional Supplemental Information Disclosure Statement (IDS)

Applicant has concurrently filed an additional supplemental IDS. Consideration of the references cited therein is respectfully requested.

Submission of Formal Drawings and Indication of Objection to Drawings

Applicants have concurrently filed a Submission of Formal Drawings. For the convenience of the Examiner, a copy of these formal drawings is enclosed. Applicant respectfully asserts that these Formal Drawings correct the informalities identified in the form PTO-948.

Rejections of Claims Under §103

Claims 1-46 were rejected over various combinations of the Kojima article, U.S. Patent No. 6,389,063 (Kanekawa), the Silicon Systems data sheet and the Zilog data sheet. Applicant traverses these rejections and has amended the claims to clarify the claimed invention.

Independent claims 1, 6, 23, 30 and 37 require that a modem and system-side line-isolation integrated circuit be configured to communicate data formatted with a synchronous protocol through an asynchronous interface. One such synchronous communication protocol is HDLC framing.

The cited references, whether taken alone or in combination, do not teach or suggest the combination of the amended claims.

The cited references, whether taken alone or in combination, do not teach or suggest a system-side integrated circuit that provides the capability of communicating data formatted using a synchronous protocol through an asynchronous interface. This claimed feature, therefore, advantageously provides an implementation that allows use of an asynchronous interface to communicate data that is formatted using a synchronous data format designed for communication through a synchronous interface, such as HDLC framing for synchronous HDLC communication. This feature of the present invention is inventive and advantageous because it allows a system that is used to communicating HDLC framed data through a synchronous interface to instead communicate this HDLC framed data through an asynchronous interface, thereby eliminating the necessity of a synchronous interface.

As noted in the Office Action, the Zilog reference discusses HDLC framing. However, as discussed below, the Zilog reference does not teach or suggest using an asynchronous interface to communicate data formatted with HDLC framing. More particularly, at page 41, the Zilog reference appears to contemplate receiving data and formatting it with HDLC framing for communication as a "synchronous data stream" and to extract data from a received "synchronous data stream" that uses HDLC framing. [Zilog, page 41, HDLC Operation.] In other words, the HDLC framed data is only contemplated for use through a synchronous interface. Thus, the Zilog reference does not appear to teach or suggest communicating HDLC formatted data through an asynchronous serial interface. It is further noted that with respect to the discussion of HDLC operation, it is unclear how the Zilog reference is using the term "host-supplied asynchronous data." It is possible that this term is referring to data received from the telephone line. What does appear to be clearly stated in the Zilog reference, however, is that the parallel and serial interfaces between the Z02201 data pump chip and the host processor provide for

"synchronous data transfer under software control." [Zilog, page 3.] Thus, with respect to page 41 and the HDLC operation, the data communicated between the Z02201 and the host processor would appear to be the "synchronous data stream" having HDLC framed data. It is further noted that unlike the current independent claims, which require a serial communication port, the Zilog reference appears to require that the synchronous parallel interface be used in HDLC mode, stating "[t]hese examples demonstrate the use of the data pump in parallel mode to transmit and receive HDLC data frames." [Zilog, page 41, top of second column.] Still further, it is noted that the serial interface between the Z02201 and the host processor is discussed on page 15 of the Zilog reference as including a transmit data clock (TCLK) and a receive data clock (RCLK), which again appears to show that the communication interface is synchronous. [Zilog, page 15, FIG. 7 and V.24 Compatible Serial Interface Port.] A timing diagram for this synchronous operation is provided on page 10 [Zilog, FIG. 5], and the synchronous data transfer functions of the TCLK and RCLK pins are discussed on pages 13-14. [Zilog, Pin Functions.] As stated above, therefore, the Zilog reference does not teach or suggest using an asynchronous serial interface to communicate data formatted with a synchronous communication protocol, such as HDLC framing.

Applicant respectfully asserts, therefore, that the cited references, either considered alone or in combination, do not anticipate or make obvious the limitations required by pending claims. Withdrawal of the rejections to these claims, therefore, is respectfully requested.

Conclusion

Applicant respectfully asserts that the pending claims are in condition for allowance. Reconsideration of the application is respectfully requested.

The Examiner is invited to contact the undersigned at the phone number indicated below with any questions or comments or to otherwise facilitate expeditious and compact prosecution of the application.

Respectfully submitted,

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**APPENDIX**
**MARKED UP VERSION OF AMENDMENTS**
**AS REQUIRED BY RULE 121**

In the Claims:

1. (Amended) A method of isolating a telephone line, comprising:

providing modem circuitry;

providing system side line isolation circuitry;

integrating the modem circuitry and system side line isolation circuitry within a single integrated circuit, the single integrated circuit configured to communicate through an isolation barrier;

providing an asynchronous serial port on the single integrated circuit, the asynchronous serial port being configured to communicate with a system-side external circuit; and

configuring the single integrated circuit to use the asynchronous serial port to transfer data [of] formatted with a synchronous modem transmission protocol between the single integrated circuit and the system-side external circuit through the asynchronous serial port.

5. (Amended) The method of claim 4, further comprising providing a transmit pin of the single integrated circuit, the receive pin and the transmit pins being asynchronous serial pins, the receive pin configured to receive modem information into the single integrated circuit from [an external interface] the external system-side circuit and the transmit pin configured to transmit modem information from the single integrated circuit to the external [interface] system-side circuit.

6. (Amended) A method of transferring information between a modem circuit and an external [interface] circuit, comprising:

providing data [of] formatted with a synchronous modem transmission protocol to an asynchronous serial pin of a modem circuit; and

using the asynchronous serial pin to transfer[ring] the data [of] formatted with the synchronous modem transmission protocol between the modem circuit and an external circuit through the asynchronous serial pin in an asynchronous manner.

7. (Amended) The method of claim 6, wherein the modem circuit [be formed within] integrated with a system side line isolation circuit.

9. (Amended) The method of claim 6, wherein the transferring comprises transmitting data from the modem circuitry to the [interface] external circuit.

18. (Amended) The method of claim 6, wherein the transferring comprises transmitting data from the [interface] external circuit to the modem circuitry.

23. (Amended) A method of transferring data between modem circuitry and an [interface] external circuit, the method comprising:

providing the modem circuitry within an integrated modem and system side line isolation circuit;

providing the integrated modem and system side line isolation circuit with an asynchronous serial pin;

providing data [of] formatted with a synchronous modem transmission protocol to the asynchronous serial pin; and

using the asynchronous serial pin to transfer[ring] the data [of] formatted with the synchronous modem transmission protocol between the modem circuitry and a system-side external circuit through the asynchronous serial pin.

26. (Amended) The method of claim 23, further comprising:

providing information on a first control pin separate from the serial pin when the modem is ready to accept additional data from the interface; and

providing information either on a second control pin separate from the serial pin or on the serial pin indicating when an end of frame has occurred.

30. (Amended) Circuitry for transferring data [of] formatted with a synchronous modem transmission protocol, comprising:

an integrated modem and line-isolation circuit;

an asynchronous serial pin, the asynchronous serial pin being an input or output pin of the integrated modem and line-isolation circuit; and

means to enable use of the asynchronous serial pin to transfer of data [of] formatted with the synchronous modem transmission protocol between the integrated modem and line-isolation circuit and an external circuit through the asynchronous serial pin.

37. (Amended) An integrated line isolation circuit, comprising:

modem circuitry and system side line isolation circuitry integrated within the line isolation circuit; and

an asynchronous serial interface pin coupled to the modem circuitry and the system side line isolation circuitry, the integrated line isolation circuit configured to use the asynchronous serial interface pin to transfer data [of] formatted with a synchronous modem transmission protocol between the line isolation circuit and a system-side external circuit through the asynchronous serial interface pin.

40. (Amended) The circuit of claim 37, further comprising:

a first control pin separate from the serial pin, information presented on the first control pin indicating when the modem is ready to accept additional data from the interface; and

wherein information indicating when an end of frame has occurred is either indicated at a second control pin separate from the serial pin or indicated within information presented on the serial pin.

44. (Amended) The circuit of claim 42, the synchronous modem transmission protocol event indicating when the modem is ready to accept additional data from the interface.